AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A memory device, comprising:

an array of [[a]] magnetic storage cells, each cell comprising a first magnetic layer, a second magnetic layer, and a dielectric in between each said first and second magnetic layers;

a first set of conductors to receive current for writing data to said magnetic storage cells; and

a second set of conductors to provide a voltage across the second set of conductors to cause current flow through at least one of the magnetic storage cells for heating said at least one magnetic storage cell when writing a bit of data to said at least one magnetic storage cell.

2. (Original) The memory device of claim 1, wherein the first set of conductors is electrically isolated from the second set of conductors within the array of magnetic storage cells.

3. (Currently Amended) The memory device of claim 1, wherein heating said at least one magnetic storage cell reduces the magnetic coercivity of at least one of the first and second magnetic layers ~~comprising~~ of the magnetic storage cell.

4. (Original) The memory device of claim 1, wherein the array of magnetic storage cells comprise spin tunneling storage cells.

5. (Original) The memory device of claim 1, wherein the array of magnetic storage cells comprise giant magnetoresistive storage cells.

6. (Original) The memory device of claim 1, wherein said array of magnetic storage cells comprise anisotropic magnetoresistive material.

7. (Original) The memory device of claim 1, wherein said array of magnetic storage cells comprise any magnetoresistive storage material.

8. (Original) The memory device of claim 1 wherein said magnetic storage cells serve as electrical heating elements.

9. (Cancelled)

10. (Original) The memory device of claim 1, wherein said second conductor set includes a heater element placed in series with at least one of the conductors of the second conductor set.

11. (Original) The memory device of claim 10, wherein said heater element is a resistive device.

12. (Currently Amended) ~~The memory device of claim 1,~~ A memory device, comprising:

an array of magnetic storage cells, each cell comprising a first magnetic layer, a second magnetic layer, and a dielectric in between each said first and second magnetic layers;

a first set of conductors to receive current for writing data to said magnetic storage cells;

a second set of conductors for heating at least one magnetic storage cell when writing a bit of data to said at least one magnetic storage cell; and

~~wherein said magnetic memory device includes~~ a heater element placed in series with the at least one ~~of the said~~ magnetic storage ~~cells~~ cell.

13. – 18. (Cancelled)

19. (Currently Amended) An electronic device comprising:
a processor;
an input device coupled to said processor;
an output device coupled to said processor;
and a memory device coupled to said processor, wherein said memory device comprises[[;]]:
an array of a magnetic storage cells, each ~~region~~ magnetic storage cell comprising a first magnetic layer, a second magnetic layer, and a dielectric in between each said first and second magnetic layers;
a first set of conductors to receive current for writing data to said magnetic storage cells; and
a second set of conductors for applying a voltage across ~~said~~ at least one magnetic storage cell for heating said at least one magnetic storage cell prior to writing a bit of data to said at least one magnetic storage cell.

20. (Original) The electronic device of claim 19, wherein the array of magnetic storage cells comprise random access memory.

21. (Original) The electronic device of claim 19, wherein said first magnetic layer has a fixed orientation of magnetization and the second layer has a non-fixed orientation.

22. (Original) The electronic device of claim 19, wherein at least one of said second set of conductors includes a resistive heating element for heating each magnetic storage cell when current flows through said heating element.

23. (Currently Amended) A magnetic storage cell comprising~~;~~:

a first magnetic layer, a second magnetic layer, and a dielectric in between said first and second magnetic layers;

a first set of conductors positioned above and below said first and second magnetic layers for writing to said magnetic storage cell; and

a second set of conductors positioned above and below said first and second magnetic layers for applying a voltage across [[a]] said magnetic storage cell for heating said ~~selected~~ magnetic storage cell prior to writing a bit of data to said magnetic storage cell and for reading the data bit that is stored on said magnetic storage cell.

24. (Original) The magnetic storage cell of claim 23, wherein said magnetic storage cell is a spin tunneling storage cell.

25. (New) The memory device of claim 1, wherein the first set of conductors is separate from the second set of conductors.

26. (New) The memory device of claim 1, wherein the first and second magnetic layers and the dielectric of the at least one magnetic storage cell and the first and second set of conductors are arranged in a stack,

wherein the second set of conductors is located between the first set of conductors in the stack.

27. (New) The memory device of claim 26, the second set of conductors to further provide a read voltage across the second set of conductors to read the at least one magnetic storage cell during a read operation.

28. (New) The memory device of claim 1, the second set of conductors to further provide a read voltage across the second set of conductors to read the at least one magnetic storage cell during a read operation.

29. (New) The electronic device of claim 19, wherein the first set of conductors is separate from the second set of conductors.

30. (New) The electronic device of claim 19, wherein the first and second magnetic layers and the dielectric of the at least one magnetic storage cell and the first and second set of conductors are arranged in a stack,
wherein the second set of conductors is located between the first set of conductors in the stack.

31. (New) The electronic device of claim 30, the second set of conductors to further provide a read voltage across the second set of conductors to read the at least one magnetic storage cell during a read operation.

32. (New) The electronic device of claim 19, the second set of conductors to further provide a read voltage across the second set of conductors to read the at least one magnetic storage cell during a read operation.

33. (New) The magnetic storage cell of claim 23, wherein the first and second magnetic layers, dielectric, first set of conductors, and second set of conductors are arranged in a stack, and
wherein the second set of conductors is located between the first set of conductors in the stack.